CLAIMS

What is claimed is:

1. A method of forming a semiconductor substrate, comprising:

etching a groove into a bulk silicon substrate;

forming a dielectric in said groove and planarizing said silicon substrate to form at least one patterned dielectric island in said silicon substrate;

forming an amorphous silicon layer on exposed portions of said silicon substrate and said at least one dielectric island;

crystallizing said amorphous silicon layer using the exposed silicon substrate as a seed, said silicon substrate having direct contact with the formed silicon layer serving as a crystal growth seeding for the crystallization process, and converting the silicon layer to crystallized silicon; and

performing a shallow trench isolation (STI) process, to form oxide isolations between devices.

2. The method according to claim 1, wherein defects in a defect zone in said substrate are removed by replacing said defects with dielectric in said STI process.

3. The method according to claim 2, wherein circuits are arranged such that

original defect zones in said substrate are used as an isolation area.

4. The method according to claim 2, wherein said performing said STI process includes using a mask, and

wherein said mask used for said STI process is designed such that original defect zones in said substrate are converted to isolations.

5. The method according to claim 1, wherein said amorphous silicon layer comprises polycrystalline silicon or microcrystalline silicon and rendered amorphous by an inert ion implantation.

6. The method according to claim 1, wherein said crystallizing comprises crystallizing through an annealing process.

7. The method according to claim 6, wherein said annealing process comprises a laser beam annealing process.

8. The method according to claim 6, wherein said annealing process comprises an ion beam annealing process.

9. The method according to claim 1, wherein said crystallized layer has a crystal orientation and structure which follow those of the underlying substrate.

10. A method of forming a substrate for mixed logic and memory applications, comprising:

forming a buried oxide layer on a single crystal silicon substrate;

performing a silicon epitaxial lateral overgrowth process using an exposed area of the silicon substrate as the crystallization seeding, to form a single crystal silicon on top of said buried oxide layer by lateral overgrowth from the exposed area of the silicon substrate; and

forming shallow trench isolations (STIs) at locations to remove imperfect silicon on said oxide layer.

11. A method of forming a substrate for mixed logic and memory applications, comprising:

forming a buried oxide layer on a single crystal silicon substrate;

forming an amorphous silicon layer over the oxide layer and silicon substrate;

annealing said amorphous silicon layer and converting said amorphous layer to a single crystalline silicon; and

forming shallow trench isolations (STIs) at locations to remove imperfect silicon on said oxide layer.

12. The method according to claim 11, wherein said substrate has a mixed bulk region and a silicon-on-insulator (SOI) region, said method further

comprising:

fabricating a logic device in the silicon-on-insulator (SOI) region.

13. The method according to claim 12, wherein said bulk region includes at least one of a memory array, a dynamic random access memory (DRAM), a static random access memory (SRAM), a flash memory, a predetermined high voltage, high power circuit, and an analog circuit.

14. The method according to claim 11, wherein said substrate has a mixed bulk region and a silicon-on-insulator (SOI) region, said method further comprising:

fabricating a memory device in the bulk silicon region.

15. The method according to claim 14, wherein said SOI region includes at least one of logic circuit, a predetermined low voltage, low power circuit, and a high performance digital circuit operating at a predetermined clock rate.

16. The method according to claim 11, wherein said forming said buried oxide layer comprises forming a groove in the silicon substrate, and filling said groove with oxide.

17. The method according to claim 11, wherein logic devices are placed in strips of silicon-on-insulator (SOI) islands which are isolated by regions

formed by the shallow trench isolation (STI) process.

18. The method according to claim 11, wherein noise-sensitive circuits are placed in strips of silicon-on-insulator (SOI) islands which are isolated by regions formed by the shallow trench isolation (STI) process.

19. The method according to claim 17, wherein said logic devices comprise P-FET and N-FET devices.

20. The method according to claim 11, wherein said substrate includes a bulk region, and

wherein thermal-sensitive circuits are placed in the bulk region such that temperature control is maximized.

21. A method of forming a substrate for mixed memory and logic applications, comprising:

forming a dielectric on a substrate;

performing an epitaxial lateral overgrowth process over the dielectric;

performing a pattern isolation operation, to form an isolation while removing a defective area; and

forming a thermal oxide to consume the silicon in an exposed area, such that a first remaining area forms a silicon-on-insulator (SOI) structure, and a second remaining area forms a bulk structure.

22. The method according to claim 21, wherein said dielectric has a thickness in a range of about 500 Å to about 3000 Å, and is patterned through a dry etch, and

wherein a corner of the patterned dielectric is rounded.

23. A method of forming a structure for mixed memory and logic applications, comprising:

processing a buried dielectric layer on a single crystal silicon substrate by depositing a dielectric and patterning said dielectric in said silicon substrate;

forming an amorphous silicon layer over the dielectric layer and the silicon substrate surface;

converting said amorphous silicon layer to a single crystalline silicon by an annealing process;

patterning said silicon surface with a nitride mask; and

oxidizing exposed silicon surfaces including locations to remove imperfect silicon on insulator layers.

24. A semiconductor device, comprising:

a bulk silicon substrate;

at least one patterned oxide island formed in said silicon substrate, said at least one island formed of a shallow groove filled with an oxide;

an amorphous silicon layer formed on exposed portions of said silicon substrate and said at least one oxide island, said amorphous silicon layer being crystallized using the exposed silicon substrate as a seed, said silicon substrate having direct contact with the formed silicon layer serving as a crystal growth seeding for the crystallization process, and converting the silicon layer to crystallized silicon; and

shallow trench isolations formed respectively between adjacent devices on said semiconductor device, wherein a portion of the silicon layer above the islands is etched to form a cavity, and a same material as said islands is formed in the cavity,

an upper surface of said trench isolations, said substrate, and said silicon layer being planarized.

25. A substrate for mixed logic and memory applications, comprising:

a single crystal silicon substrate forming a bulk silicon region;

a buried oxide layer on the single crystal silicon substrate forming a silicon-on-insulator (SOI) region;

an amorphous silicon layer formed substantially over the oxide layer; and

shallow trench isolations (STIs) formed at predetermined locations to remove defects on the SOI region.

26. The substrate according to claim 25, further comprising a logic device

formed in the silicon-on-insulator (SOI) region.

27. The substrate according to claim 25, further comprising a memory device positioned in the bulk silicon region.

28. A semiconductor device, comprising:

a bulk silicon substrate;

at least one patterned oxide island formed in said silicon substrate, said at least one island formed of a shallow groove filled with an oxide;

a SiGe layer formed on exposed portions of said silicon substrate and said at least one oxide island, said SiGe layer being crystallized using the exposed silicon substrate as a seed, said silicon substrate having direct contact with the formed SiGe layer serving as a crystal growth seeding for the crystallization process, and converting the SiGe layer to crystallized silicon; and

shallow trench isolations formed respectively between adjacent devices on said substrate, wherein a portion of the SiGe layer above the islands is etched to form a cavity, and a same material as said islands is formed in the cavity, an upper surface of said trench isolations, said substrate, and said SiGe layer being planarized,

wherein said SiGe layer is at least partially positioned on a bulk region of said substrate and a silicon-on-insulator (SOI) portion of said substrate.

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